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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/725,898	12/01/2003	San Wong	174/297	3367

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EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 05/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/725,898	WONG ET AL.	
	Examiner	Art Unit	
	Cynthia Britt	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-25 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-25 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 27 December 2005 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 12-27-05.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-25 are presented for examination.

Drawings

The drawings are objected to because descriptive labels other than numerical are needed for figures 1 elements 100, 120, 122, and 104. See 37 CFR 1.84(o).

The drawings are objected to because Figure 1 element 114 should be "comparator".

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-12 and 15-25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 1, lines 1 and 2 state, " A bit error rate tester that tests the bit error rate of an interface,..."it is unclear to the examiner how an interface would have a rate. Therefore, the examiner will assume that applicant is testing the error rate of the data that is sent through the interface.

It is also unclear to the examiner what applicant is intending to claim with respect to the "comparison data" and "test data". As the claim reads, it is unclear if the comparison data is the result of the comparison with expected data or if the comparison is the expected data as a result of the testing and/or if the "test data" is actually the data obtained as a result of the test or if it is the actual data stream used to test the interface. This must be clarified in order for the examiner to fully understand what applicant is intending to claim as his invention.

As per claim 3, it is unclear to the examiner how a circuit would be implemented in a programmable logic device without using programmable logic circuitry and would therefore be inherent.

As per claims 9 and 10, the examiner would like to point out that whether the interface is internal or external to the device the functional equivalency would be unchanged.

As per claim 11, it is unclear to the examiner if the statement "wherein the first memory and the second memory are the same" is intended to mean that there is only a single physical device or whether the applicant intends to claim that the type of memory is the same (i.e. RAM ROM etc.). Applicant should note that the independent claim recites 2 memories; therefore if applicant intends a single physical memory, care should be taken not to contradict the independent claim.

As per claim 12, the statement "wherein the test data and the comparison data are the same" is also unclear in that if the data is the same data coming from the same memory it is unclear how the connections recited in the independent claim would be achieved.

Claims 2-12, and 15-17 are dependent on independent claim 1, and therefore inherit the 35 USC 112 second paragraph deficiencies of the independent claim 1 and may not be further considered on the merits.

As per claim 13, it is unclear to the examiner what applicant is intending to claim with respect to the "comparison data" and "test data". As the claim reads, it is unclear if the comparison data is the result of the comparison with expected data or if the comparison is the expected data as a result of the testing and/or if the "test data" is actually the data obtained as a result of the test or if it is the actual data stream used to

test the interface. This must be clarified in order for the examiner to fully understand what applicant is intending to claim as his invention.

As per claim 18, the phrase "synchronizing a comparison of incoming values with comparison values" is unclear for the same reasons as stated above because it is unclear from reading the claim what the difference is between the two.
The statement "comparing an incoming value to a comparison value" is unclear for the same reasons.

As per claim 21, step (3) states "repeating (1) and (2) until a predetermined condition is met." However, claim 21 is dependent on claim 18 and both claims recite a (1) and a (2). Therefore it is unclear which of the (1) or (2) is being referred to in step (3).

As per claim 19-21, these are dependent on independent claim 18, and therefore inherit the 35 USC 112 second paragraph deficiencies of the independent claim 18 and may not be further considered on the merits.

As per claim 22, " A method for testing the bit error of an interface,..."it is unclear to the examiner how an interface would have a rate. Therefore, the examiner will assume that applicant is testing the error rate of the data that is sent through the interface. The phrase "comparing the incoming data to the comparison data is also unclear. As the claim reads, it is unclear if the comparison data is the result of the comparison with expected data or if the comparison is the expected data as a result of the testing. Clarification of this point within the claim language is required.

As per claims 23 and 24, the examiner would like to point out that whether the interface is internal or external to the device the functional equivalency would be unchanged.

As per claim 25, "comparing the incoming data to the comparison data is unclear.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –333
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 13 and 14 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Appleton et al. U.S. Patent No.6,628,621.

Appleton et al. teaches the claimed bit error rate tester (BERT) system which is configured as a field programmable gate array that emulates multiple independent BERT generators. The BERT generators produce test frames containing test pattern codes associated with respectively different time division multiplexed (TDM) digital communication channels, that are not necessarily mutually contiguous within a plurality of TDM timeslots of a network communication frame serving digital communication circuits. A framing unit assembles the test code patterns into a test frame and transmits the test frame over a serial network interface to a plurality of digital channel units of a

channel bank. The framing unit also interfaces contents of test code patterns within test frames returned from the channel units over the serial network interface with a plurality of data channel-specific virtual BERT receivers, associated with respective digital communication channels. A bit error processor determines errors in the contents of the test code patterns within returned test frames. (Abstract)

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 7,032,139 Iryami et al.

This patent teaches a bit error rate tester that may operate on network paths having devices that add or drop idles within a transmitted bit sequence. In particular, the bit sequence determines whether a received bit sequence is synchronized. If the received sequence is not synchronized or if a certain event/threshold is reached, then the bit error rate tester re-synchronizes the sequence prior to analysis. Also, the bit error rate detector is able to operate on high-speed networks and provide bit granularity measurements.

"How Programmable Logic Works" by Michael Barr published June 1999, Embedded Systems Programming on pages 75-84

This paper teaches that FPGAs can be used to implement almost any hardware device and that attribute is what makes the FPGA desirable in the design area.

U.S. Pre-grant Publication 2005/0050190 A1 Dube

This publication discloses flexibly configurable network diagnostic modules that can implement any of a plurality of network diagnostic functions. A network diagnostic module receives an indication that a selected network diagnostic function (e.g., network analyzer, jammer, generator, bit error rate tester, etc.) is to be implemented. The network diagnostic module receives a bit file with instructions or data for implementing the selected network diagnostic function at one or more ports. The network diagnostic module identifies a programmable logic module (e.g., a Field-Programmable Gate Array ("FPGA")) that controls the one or ports. The network diagnostic module loads a portion of the bit file at the identified programmable logic module to cause the programmable logic module and the one or more ports to interoperate to implement the selected network diagnostic function.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cynthia Britt
Examiner
Art Unit 2138